WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory comprising:

a memory cell section including a memory cell;

a bit line connected to said memory cell section; and

a data circuit connected to said bit line, said data circuit temporarily storing program / read data having two ore more bits;

wherein said data circuit includes a first capacitor storing first data, and a first latch circuit storing second data.

2. A nonvolatile semiconductor memory comprising:

a memory cell section including a memory cell storing data having three or more values;

a bit line connected to said memory cell section; and

a data circuit connected to said bit line, said data circuit temporarily storing program / read data having two or more bits;

wherein said data circuit includes a first capacitor storing first data, and a first latch circuit storing second data.

3. A nonvolatile semiconductor memory comprising:

a memory cell section including a memory cell storing data having three or more values;

a bit line connected to said memory cell section; and

a data circuit connected to said bit line, said data circuit temporarily storing program / read data having two or more bits;

wherein said data circuit includes a first capacitor and a first latch circuit, and

a program operation to said memory cell is executed based on a first data stored in said first capacitor and second data stored in said first latch circuit.

4. A nonvolatile semiconductor memory comprising:

a memory cell section including a memory cell storing data having three or more values;

a bit line connected to said memory cell section; and

a data circuit connected to said bit line, said data circuit temporarily storing program / read data having two or more bits;

wherein said data circuit includes a first capacitor and a first latch circuit, and

a program operation to said memory cell is executed based on first data read from said memory cell and stored in said first capacitor and second data input from outside the chip, on which said memory cell section is formed, and stored in said first latch circuit.

5. A nonvolatile semiconductor memory comprising:

a memory cell section including a memory cell

storing data having three or more values;

a bit line connected to said memory cell section; and

a data circuit connected to said bit line, said data circuit temporarily storing program / read data having two or more bits;

wherein said data circuit includes a first capacitor and a first latch circuit,

a first program operation and a second program operation are carried out to store first data and second data in said memory cell,

in said first program operation, said first data is programmed to said memory cell based on said first data stored in said first latch circuit, and

in said second program operation, said first and second data are stored in said memory cell based on said second data stored in said first latch circuit and said first data read from said memory cell and stored in said first capacitor.

6. A nonvolatile semiconductor memory comprising:

a memory cell section storing data having n values, where n is a natural number of not higher than 3, said memory cell including a memory cell set at a "1" state in which the memory cell has a first threshold level, a "2" state in which the memory cell has a second threshold level, ··· and an "n" state in which the memory cell has an n-th threshold level according to a

value of said data;

a bit line connected to said memory cell section; and

a data circuit connected to said bit line, said data circuit temporarily storing program / read data having two bits or more;

wherein said data circuit includes a first capacitor and a first latch circuit,

a first program operation and a second program operation are conducted to store first data and second data in said memory cell,

in said first program operation, said memory cell is set at one of said "1" state, said "2" state, ··· and an "m" state, where m < n, based on said first data stored in said first latch circuit, and

in said second program operation, said memory cell is set at one of said "1" state, said "2" state, ··· and a "k" state, where m > k > n, based on said second data stored in said first latch circuit and said first data read from said memory cell and stored in said first capacitor.

7. A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a second memory cell section including a second memory cell;

a bit line connected to said first and second

memory cell sections; and

a data circuit connected to said bit line, said data circuit temporarily storing program / read data having two bits or more;

wherein said data circuit includes a first capacitor storing first data written into or read from said first memory cell, and a second latch circuit storing second data written into or read from said second memory cell.

8. A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a second memory cell section including a second memory cell;

a bit line connected to said first and second memory cell sections; and

a data circuit connected to said bit line, said data circuit temporarily storing program / read data having two bits or more;

wherein said data circuit includes a first capacitor and a first latch circuit,

in a second program operation to said second memory cell, said first capacitor stores first data, said second program operation conducted based on second data stored in said first latch circuit;

in a first program operation to said first memory cell, said first data stored in said first capacitor is

transferred to said first latch circuit, said first program operation conducted based on said first data stored in said first latch circuit.

9. The nonvolatile semiconductor memory according to claim 1, further comprising a refresh circuit configured to refresh data stored in said first capacitor.

10. The nonvolatile semiconductor memory according to claim 9, wherein

said refresh circuit transfers the data stored in said first latch circuit to said bit line; and

said refresh circuit refreshes the data stored in said first capacitor using said first latch circuit while said data stored in said first latch circuit is held by said bit line, and then transfers said data held by said bit line to said first latch circuit.

11. The nonvolatile semiconductor memory according to claim 10, wherein said data stored in said first capacitor is refreshed while a program pulse is being supplied to said memory cell or after supply of said program pulse ends.

12. The nonvolatile semiconductor memory according to claim 1, wherein said memory cell is one of a plurality of memory cells constituting an NAND cell unit.

13. The nonvolatile semiconductor memory according to claim 2, further comprising a refresh circuit

configured to refresh data stored in said first capacitor.

14. The nonvolatile semiconductor memory according to claim 13, wherein

said refresh circuit transfers the data stored in said first latch circuit to said bit line; and

said refresh circuit refreshes the data stored in said first capacitor using said first latch circuit while said data stored in said first latch circuit is held by said bit line, and then transfers said data held by said bit line to said first latch circuit.

15. The nonvolatile semiconductor memory according to claim 14, wherein said data stored in said first capacitor is refreshed while a program pulse is being supplied to said memory cell or after supply of said program pulse ends.

16. The nonvolatile semiconductor memory according to claim 2, wherein said memory cell is one of a plurality of memory cells constituting an NAND cell unit.

17. The nonvolatile semiconductor memory according to claim 3, further comprising a refresh circuit configured to refresh data stored in said first capacitor.

18. The nonvolatile semiconductor memory according to claim 17, wherein

said refresh circuit transfers the data stored in

said first latch circuit to said bit line; and

said refresh circuit refreshes the data stored in said first capacitor using said first latch circuit while said data stored in said first latch circuit is held by said bit line, and then transfers said data held by said bit line to said first latch circuit.

19. The nonvolatile semiconductor memory according to claim 18, wherein said data stored in said first capacitor is refreshed while a program pulse is being supplied to said memory cell or after supply of said program pulse ends.

20. The nonvolatile semiconductor memory according to claim 3, wherein said memory cell is one of a plurality of memory cells constituting an NAND cell unit.

21. The nonvolatile semiconductor memory according to claim 4, further comprising a refresh circuit configured to refresh data stored in said first capacitor.

22. The nonvolatile semiconductor memory according to claim 21, wherein

said refresh circuit transfers the data stored in said first latch circuit to said bit line; and

said refresh circuit refreshes the data stored in said first capacitor using said first latch circuit while said data stored in said first latch circuit is held by said bit line, and then transfers said data

held by said bit line to said first latch circuit.

23. The nonvolatile semiconductor memory according to claim 22, wherein said data stored in said first capacitor is refreshed while a program pulse is being supplied to said memory cell or after supply of said program pulse ends.

24. The nonvolatile semiconductor memory according to claim 4, wherein said memory cell is one of a plurality of memory cells constituting an NAND cell unit.

25. The nonvolatile semiconductor memory according to claim 5, further comprising a refresh circuit configured to refresh data stored in said first capacitor.

26. The nonvolatile semiconductor memory according to claim 25, wherein

said refresh circuit transfers the data stored in said first latch circuit to said bit line; and

said refresh circuit refreshes the data stored in said first capacitor using said first latch circuit while said data stored in said first latch circuit is held by said bit line, and then transfers said data held by said bit line to said first latch circuit.

27. The nonvolatile semiconductor memory according to claim 26, wherein said data stored in said first capacitor is refreshed while a program pulse is being supplied to said memory cell or after supply of said

program pulse ends.

28. The nonvolatile semiconductor memory according to claim 5, wherein said memory cell is one of a plurality of memory cells constituting an NAND cell unit.

29. The nonvolatile semiconductor memory according to claim 6, further comprising a refresh circuit configured to refresh data stored in said first capacitor.

30. The nonvolatile semiconductor memory according to claim 29, wherein

said refresh circuit transfers the data stored in said first latch circuit to said bit line; and

said refresh circuit refreshes the data stored in said first capacitor using said first latch circuit while said data stored in said first latch circuit is held by said bit line, and then transfers said data held by said bit line to said first latch circuit.

31. The nonvolatile semiconductor memory according to claim 30, wherein said data stored in said first capacitor is refreshed while a program pulse is being supplied to said memory cell or after supply of said program pulse ends.

32. The nonvolatile semiconductor memory according to claim 6, wherein said memory cell is one of a plurality of memory cells constituting an NAND cell unit.

33. The nonvolatile semiconductor memory according to claim 7, further comprising a refresh circuit configured to refresh data stored in said first capacitor.

34. The nonvolatile semiconductor memory according to claim 33, wherein

said refresh circuit transfers the data stored in said first latch circuit to said bit line; and

said refresh circuit refreshes the data stored in said first capacitor using said first latch circuit while said data stored in said first latch circuit is held by said bit line, and then transfers said data held by said bit line to said first latch circuit.

35. The nonvolatile semiconductor memory according to claim 34, wherein said data stored in said first capacitor is refreshed while a program pulse is being supplied to said memory cell or after supply of said program pulse ends.

36. The nonvolatile semiconductor memory according to claim 7, wherein said memory cell is one of a plurality of memory cells constituting an NAND cell unit.

37. The nonvolatile semiconductor memory according to claim 8, further comprising a refresh circuit configured to refresh data stored in said first capacitor.

38. The nonvolatile semiconductor memory according

to claim 37, wherein

said refresh circuit transfers the data stored in said first latch circuit to said bit line; and

said refresh circuit refreshes the data stored in said first capacitor using said first latch circuit while said data stored in said first latch circuit is held by said bit line, and then transfers said data held by said bit line to said first latch circuit.

39. The nonvolatile semiconductor memory according to claim 38, wherein said data stored in said first capacitor is refreshed while a program pulse is being supplied to said memory cell or after supply of said program pulse ends.

40. The nonvolatile semiconductor memory according to claim 8, wherein said memory cell is one of a plurality of memory cells constituting an NAND cell unit.

41. A nonvolatile semiconductor memory comprising:

a memory cell section including a memory cell;

a first signal line connected to said memory cell section;

a data circuit temporarily storing program / read data; and

a first switching circuit connected between said first signal line and said data circuit;

wherein said first switching circuit is turned off, whereby said first signal line is electrically

disconnected from said data circuit and said program / read data is held by said first signal line.

42. A nonvolatile semiconductor memory comprising:

a memory cell section including a memory cell;

a first signal line connected to said memory cell section;

a data circuit temporarily storing program / read data; and

a first switching circuit connected between said first signal line and said data circuit;

wherein said first switching circuit is turned off, whereby said first signal line is electrically disconnected from said data circuit and said program / read data is held by said first signal line without being held by said data circuit.

43. The nonvolatile semiconductor memory according to claim 41, wherein

said first switching circuit is turned off while a program voltage is supplied to said memory cell, whereby said first signal line is electrically disconnected from said data circuit and program data is held by said first signal line.

44. The nonvolatile semiconductor memory according to claim 42, wherein

said first switching circuit is turned off while a program voltage is supplied to said memory cell, whereby said first signal line is electrically

disconnected from said data circuit and program data is held by said first signal line.

45. A nonvolatile semiconductor memory comprising:

a memory cell section including a memory cell;

a first signal line connected to said memory cell section;

a data circuit temporarily storing program / read data; and

a first switching circuit connected between said first signal line and said data circuit;

wherein said first switching circuit is turned off while a program voltage is supplied to said memory cell, whereby said first signal line is electrically disconnected from said data circuit; and

said program / read data is held by said first signal line, said first switching circuit is turned on after said program voltage is supplied to said memory cell, whereby said data circuit is electrically connected to said first signal line and said program data held by said first signal line is transferred to said data circuit.

46. A nonvolatile semiconductor memory comprising:

a memory cell section including a memory cell;

a first signal line connected to said memory cell section;

a data circuit temporarily storing program / read data; and

a first switching circuit connected between said first signal line and said data circuit;

wherein said first switching circuit is turned off while a program voltage is supplied to said memory cell, whereby said first signal line is electrically disconnected from said data circuit;

said program / read data is held by said first signal line, said first switching circuit is turned on after said program voltage is supplied to said memory cell, whereby said data circuit is electrically connected to said first signal line and said program data held by said first signal line is transferred to said data circuit; and

a verify read operation to verify whether said memory has been sufficiently programmed, is carried out using said program data stored in said data circuit.

47. A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a second memory cell section including a second memory cell;

a first signal line connected to said first memory cell section;

a second signal line connected to said second memory cell section; and

a data circuit connected to said first and second signal lines;

wherein first program / read data of said first memory cell is temporarily stored in said data circuit, and second program / read data of said second memory cell is held by said second signal line.

48. A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a second memory cell section including a second memory cell;

a first signal line connected to said first memory cell section;

a second signal line connected to said second memory cell section; and

a data circuit connected to said first and second signal lines;

wherein

said first and second memory cells are programmed substantially simultaneously; and

while a program voltage is supplied to said second memory cell, program data of said second memory cell is held by said second signal line, and while said program voltage is supplied to said second memory cell, a verify read operation to verify whether said first memory cell has been programmed sufficiently, is carried out by said data circuit.

49. A nonvolatile semiconductor memory comprising:

a first memory cell section including a first

memory cell;

a second memory cell section including a second memory cell;

a first signal line connected to said first memory cell section;

a second signal line connected to said second memory cell section; and

a data circuit connected to said first and second signal lines;

wherein

said first and second memory cells are programmed substantially simultaneously;

while a program voltage is supplied to said second memory cell, program data of said second memory cell is held by said second signal line, and while said program voltage is supplied to said second memory cell, a verify read operation to verify whether said first memory cell has been programmed sufficiently, is carried out by said data circuit; and

while said program voltage is supplied to said first memory cell, program data of said first memory cell is held by said first signal line, and while said program voltage is supplied to said first memory cell, a verify read operation to verify whether said second memory cell has been programmed sufficiently, is carried out by said data circuit.

50. A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a second memory cell section including a second memory cell;

a first signal line connected to said first memory cell section;

a second signal line connected to said second memory cell section; and

a data circuit connected to said first and second signal lines;

wherein

said first and second memory cells are programmed substantially simultaneously;

while a program voltage is supplied to said second memory cell, program data of said second memory cell is held by said second signal line, and while said program voltage is supplied to said second memory cell, the program data of said first memory cell held by said first signal line is transferred to said data circuit and a verify read operation to verify whether said first memory cell has been programmed sufficiently, is carried out by said data circuit;

while said program voltage is supplied to said first memory cell, program data of said first memory cell is held by said first signal line, and while said program voltage is supplied to said first memory cell, the program data of said second memory cell held by

said second signal line is transferred to said data circuit and a verify read operation to verify whether said second memory cell has been programmed sufficiently, is carried out by said data circuit.

51. The nonvolatile semiconductor memory according to claim 47, wherein

said first memory cell and said second memory cell are connected to different word lines.

52. The nonvolatile semiconductor memory according to claim 48, wherein

said first memory cell and said second memory cell are connected to different word lines.

53. The nonvolatile semiconductor memory according to claim 49, wherein

said first memory cell and said second memory cell are connected to different word lines.

54. The nonvolatile semiconductor memory according to claim 50, wherein

said first memory cell and said second memory cell are connected to different word lines.

55. A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a first signal line connected to said first memory cell section;

a second signal line; and

a data circuit connected to said first and second

signal lines, said data circuit temporarily storing program / read data;

wherein

said program / read data of said first memory cell is held by said second signal line.

56. A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a first signal line connected to said first memory cell section;

a second signal line; and

a data circuit connected to said first and second signal lines, said data circuit temporarily storing program / read data;

wherein

while a program voltage is supplied to said first memory cell, program data of said first memory cell is held by at least one of said first and second signal lines;

after said program voltage is supplied to said first memory cell, said data circuit is electrically connected to said second signal line and the program data of said first memory cell held by said second signal line is transferred to said data circuit; and

a verify read operation to verify whether said first memory cell has been sufficiently programmed, is carried out using said program data stored in said data

circuit.

57. A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a first signal line connected to said first memory cell section;

a second signal line;

a third memory cell section including a third memory cell;

a third signal line connected to said third memory cell section;

a fourth signal line; and

a data circuit connected to said first, second, third and fourth signal lines, said data circuit temporarily storing program / read data of at least one of said first and third memory cells,

wherein

said first and third memory cells are programmed substantially simultaneously, program data of said first memory cell is held by at least one of said first and second signal lines, and program data of said third memory cell is held by at least one of said third and fourth signal lines while a program voltage is supplied to said first and second memory cells;

a verify read operation to verify whether said first memory cell has been sufficiently programmed, is carried out by said data circuit, and program data of

said third memory cell is held by said fourth signal line while conducting the verify read operation of said first memory cell; and

said data circuit and said fourth signal line are electrically connected to each other, after the program data of said third memory cell held by said fourth signal line is transferred to said data circuit, a verify read operation to verify whether said third memory cell has been sufficiently programmed, is carried out using the program data of said third memory cell held by said data circuit, and while conducting a verify read operation of said third memory cell, the program data of said first memory cell is held by said second signal line.

58. The nonvolatile semiconductor memory according to claim 57, wherein

said first and third memory cells are connected to a same word line.

59. The nonvolatile semiconductor memory according to claim 55, wherein

while said program / read data is held by said first or second signal line, a potential of a signal line adjacent to said first or second signal line is set at a fixed potential.

60. The nonvolatile semiconductor memory according to claim 59, wherein

said fixed potential is a ground potential or a

power supply potential.

61. The nonvolatile semiconductor memory according to claim 55, wherein

said first and second signal lines are bit lines.

62. The nonvolatile semiconductor memory according to claim 56, wherein

while said program / read data is held by said first or second signal line, a potential of a signal line adjacent to said first or second signal line is set at a fixed potential.

63. The nonvolatile semiconductor memory according to claim 62, wherein

said fixed potential is a ground potential or a power supply potential.

64. The nonvolatile semiconductor memory according to claim 56, wherein

said first and second signal lines are bit lines.

65. The nonvolatile semiconductor memory according to claim 57, wherein

while said program / read data is held by said first, second, third or fourth signal line, a potential of a signal line adjacent to said first, second, third or fourth signal line is set at a fixed potential.

66. The nonvolatile semiconductor memory according to claim 62, wherein

said fixed potential is a ground potential or a power supply potential.

67. The nonvolatile semiconductor memory according to claim 56, wherein

said first, second, third and fourth signal lines are bit lines.

68. A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a second memory cell section including a second memory cell;

a bit line connected to said first and second memory cell sections; and

a data circuit connected to said bit line, said data circuit temporarily storing program / read data;

wherein said data circuit includes a first storage means for storing data written into or read from said first memory cell, and a second storage means for storing data written into or read from said second memory cell.

69. A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a second memory cell section including a second memory cell;

a bit line connected to said first and second memory cell sections; and

a data circuit connected to said bit line, said data circuit temporarily storing program / read data;

wherein

said data circuit includes first and second storage means;

if said second memory cell is programmed, said first storage means stores first data and said second memory cell is programmed based on second data stored in said second storage means; and after second memory cell has been programmed, said first data held by said first storage means is transferred to said second storage means; and

said first memory cell is programmed based on said first data stored in said second storage means.

70. The nonvolatile semiconductor memory according to claim 68, wherein

said first storage means is a capacitor, and said second storage means is a latch circuit.

71. The nonvolatile semiconductor memory according to claim 69, wherein

said first storage means is a capacitor, and said second storage means is a latch circuit.

72. The nonvolatile semiconductor memory according to claim 68, wherein

both of said first and second storage means are latch circuits.

73. The nonvolatile semiconductor memory according to claim 69, wherein

both of said first and second storage means are

latch circuits.

74. The nonvolatile semiconductor memory according to claim 68, wherein

said first and second memory cells are connected to different word lines.

75. The nonvolatile semiconductor memory according to claim 69, wherein

said first and second memory cells are connected to different word lines.

76. The nonvolatile semiconductor memory according to claim 41, 42, 45 or 46, wherein

while said program / read data is held by said first signal line, a potential of a signal line adjacent to said first signal line is set at a fixed potential.

77. The nonvolatile semiconductor memory according to claim 76, wherein

said fixed potential is a ground potential or a power supply potential.

78. The nonvolatile semiconductor memory according to claim 41, 42, 45 or 46, wherein

said first signal line is a bit line.

79. The nonvolatile semiconductor memory according to claim 47, 48, 49 or 50, wherein

while said program / read data is held by said first or second signal line, a potential of a signal line adjacent to said first or second signal line is

set at a fixed potential.

80. The nonvolatile semiconductor memory according to claim 79, wherein

said fixed potential is a ground potential or a power supply potential.

81. The nonvolatile semiconductor memory according to claim 47, 48, 49 or 50, wherein

said first and second signal lines are bit lines.